



# INDUSTRY STANDARD PANELS

## 13.3", 14.1" and 15.0"

### Mounting and Top Level Interface Requirements

Version 1  
Oct, 1999

#### Purpose

To establish a set of displays with standard dimensions and interface characteristics so that both the notebook and panel supplier industries will be able to manage the volatile LCD supply and demand in an easier fashion. This effort will enable panels from various LCD suppliers to be used in most notebooks (*or other products utilizing these standard panels*) that are designed around these Standard Panels without having to change either the notebook/product tooling or the LCD module tooling.

#### Summary

To date, the notebook and panel industry has been plagued by an overabundance of unique/custom designs from the many LCD suppliers in the industry. This has in turn, forced the notebook OEM's and other end-product users to change their packaging, interface design, and tooling literally every time a new panel supplier or module has been used. This leads to schedule slippage's, missed market opportunities, and logistic and product obsolescence problems. Similarly, many times this problem has blocked some LCD manufacturers from being considered as a potential supplier due to the magnitude of changes that their design would force on the notebook end product. As more panel suppliers come on line in the near future, this style of independent designs would only increase this problem for both the notebook OEM's as well as the LCD suppliers. In an attempt to lessen this problem, these requirements are being established with the aid of both notebook OEM's and LCD panel suppliers.

# STANDARD PANELS WORKING GROUP



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## Support for this Standard

The Standard Panel Working Group, which consists of many of the major notebook suppliers, in conjunction with many of the leading LCD suppliers, has established these mechanical and electrical requirements defined herein. These requirements have been refined through a number of proposal/feedback review cycles with these suppliers.

*This document is intended as a reference document only for both notebook OEM's and panel suppliers. Users of this document should not base final end-product designs (notebook or other) on this document, but instead should utilize the display supplier's detailed drawings and specifications for full documentation.*



## 1. OVERVIEW

### 1.1 Summary.

This document defines selected electrical interface requirements and mechanical dimensions for a series of industry compatible XGA resolution (1024x768) LCD panels. Through the DDC and EEDID interface, it also provides graphics controller BIOS and driver support, and supports Microsoft PC99 and future PCxxxx requirements.

### 1.2 Background.

With most panels used in portable computer designs today, the notebook OEM has to have different interface cables, plastic or magnesium enclosures, bezels, bracket assemblies, and EMI shields for every panel used. For each of these parts, there are associated tooling changes required and schedule impacts relative to these tooling changes, to support the use of the different panels. Additionally, the associated documentation and logistics impacts for these different configurations are staggering. Many times these changes, and schedule impacts that would be caused by these changes, eliminates many panel suppliers from being considered as potential 2<sup>nd</sup> sources.

### 1.3 Standard Objectives.

This document establishes common panels for the three display sizes that enables any Standard Panel to be mounted in any system that has been designed to accept the maximum size Standard Panel. The Standard Panel method of dimensioning has been developed to allow panel suppliers a method of providing product differentiation and still meet the intent of transparent usage across different platforms.

Additionally, with the various requirements of PC99 and future PCxxxx versions, the incorporation of EEDID will allow transparent usage with minimum changes to system BIOS or drivers. The end objective is to specify panel timing requirement so that no BIOS or driver changes are required with the use of a new panel.

## 2. REFERENCE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. The user of this document is advised to ensure they have the latest versions of these reference standards and documents.

- VESA Display Data Channel Standard, DDC2B
- VESA Enhanced Extended Display Identification Data, (*currently in proposal stage Ver. A, Draft 11*)
- Philips I<sup>2</sup>C Bus Specification - Data Handbook I<sup>2</sup>C Peripherals for Microcontrollers 1/92
- TIA/EIA-644 ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTERFACE CIRCUITS
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## 3. SYSTEM ELECTRICAL INTERFACE REQUIREMENTS

The panels electrical interface to the system consists of 2 physical electrical interfaces comprising of the Display Data Channel interface, and the system power and LVDS interface which encodes the R-G-B data and timing/control signals.

### 3.1 Display Data Channel Requirements.

To support notebook-level transparent 2<sup>nd</sup> source capability and the requirements of Microsoft's PCxxxx requirements, the panels shall support I<sup>2</sup>C-based Display Data Channel communications. The only level of support required is DDC2B, compatibility with earlier DDC versions is not supported. The Display Data Channel serial interface shall transmit the Enhanced Extended Display Identification Data (EEDID) containing panel specific data.

#### 3.1.1 DDC2B Physical Layer Electrical Requirements.

The DDC interface shall support the full I<sup>2</sup>C interface of DDC2B requirements for signals and timing with the exception that the +5VDC monitor interface supply voltage shall be replaced with +3.3VDC.

#### 3.1.2 EDID Logical Layer Requirements.

This standard only supports VESA Enhanced EDID Structure 1.3. All data fields of structure 1.3 are required to be supported with the exception of ID serial number, Week of Manufacturer, and Year of Manufacturer fields which are optional. It is anticipated, that in the near future, as the panel suppliers develop real-time data gathering capabilities on their factory floor, that these three fields will then be implemented as well.

### 3.2 Logic Power and Data/Control Interface.

#### 3.2.1 Interface Connector Requirements.

The module interface connector shall be the JAE **FI-SEB20P-HFxxxx**, JAE **FI-SE20P-HFxxxx** or equivalent. The connector keep-out area for the module, shall be designed to support insertion of either a wire-crimp style connector, or the wider flex-cable style connector. Connector keying relative to pin 1 designation shall be as shown in JAE data sheets.

#### 3.2.2 Interface Signal Definition.

The interface connector pin assignments are listed in Table 1.

#### 3.2.3 Power Sequencing Requirements.

To prevent a latch-up or DC operation of the LCD, the panel shall support the following logic power and data/control signal sequencing of Figure 1.

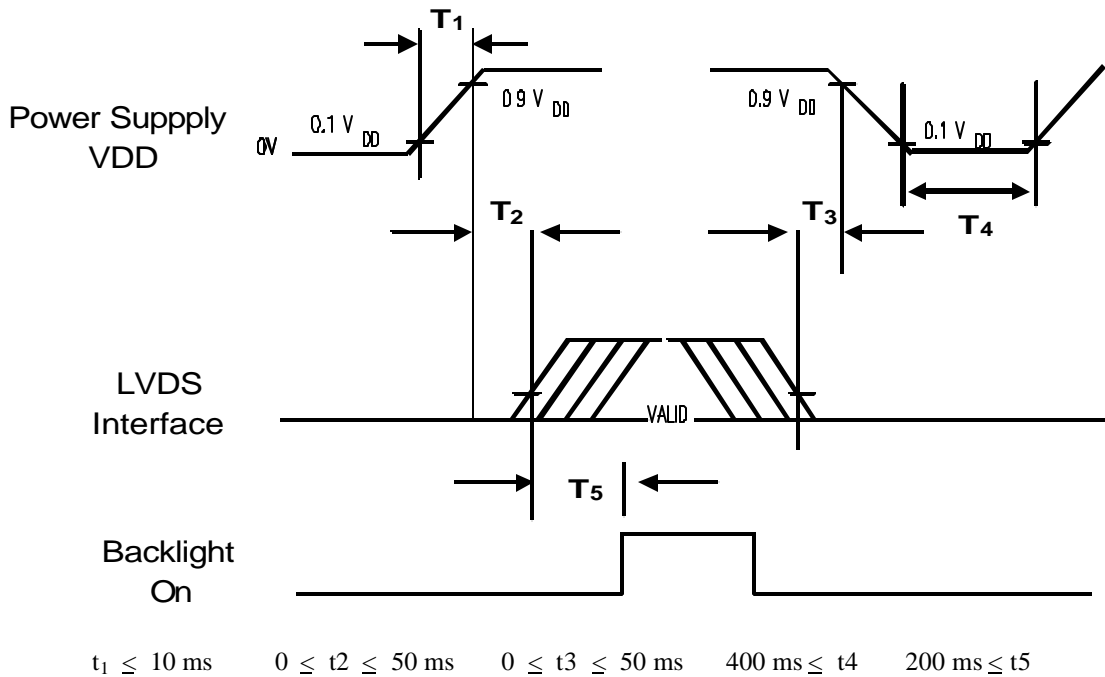


**TABLE 1  
INTERFACE CABLE PIN ASSIGNMENTS**

<b>PIN NO.</b>	<b>SYMBOL</b>	<b>FUNCTION</b>
1	VDD	Power Supply, 3.3 V (typical)
2	VDD	Power Supply, 3.3 V (typical)
3	VSS	Ground
4	VSS	Ground
5	Rin0 -	LVDS Receiver Signal (-)
6	Rin0 +	LVDS Receiver Signal (+)
7	VSS	Ground
8	Rin1 -	LVDS Receiver Signal (-)
9	Rin1 +	LVDS Receiver Signal (+)
10	VSS	Ground
11	Rin2 -	LVDS Receiver Signal (-)
12	Rin2 +	LVDS Receiver Signal (+)
13	VSS	Ground
14	CLK -	Clock Signal (-)
15	CLK +	Clock Signal (+)
16	VSS	Ground
17	V <sub>EDID</sub>	DDC 3.3V power
18	NC	Reserved for supplier test point
19	Clk <sub>EDID</sub>	DDC Clock
20	DATA <sub>EDID</sub>	DDC Data



**FIGURE 1  
LOGIC POWER AND LVDS SIGNALS SEQUENCING DIAGRAM**



**3.2.4 LVDS Data and Control Signal Interface.**

The modules LVDS signals interface shall meet requirements of TIA/EIA-644.

**3.2.4.1 LVDS Termination Impedance.**

The LVDS differential signals line-to-line termination impedance  $Z_T$ , shall be  $100 \pm 1$  ohms.

**3.2.5 Backlight Electrical Interface.**

The panel-side backlight interface cable shall be terminated into a JST BHSR-02VS-1 as the recommended connector, or a JST BHTR-02VS as an alternative choice. The lamp wires exiting the panel shall be sufficiently protected so that normal movement of these wires during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in Table 2.

**TABLE 2  
BACKLIGHT ELECTRICAL INTERFACE**

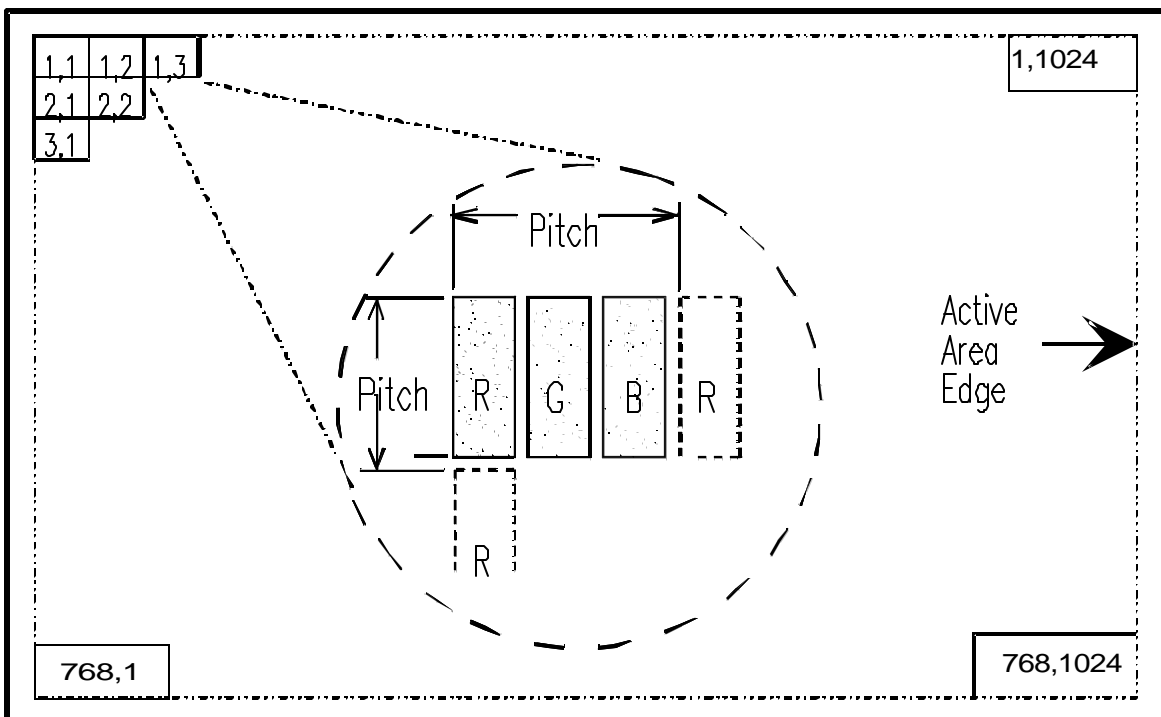
PIN NO.	SIGNAL	LEVEL	FUNCTION
1	V <sub>CFL</sub>	AC	Power Supply for CFL
2	Gnd Rtn	~ GND	Power return for CFL



#### 4. MECHANICAL INTERFACE REQUIREMENTS

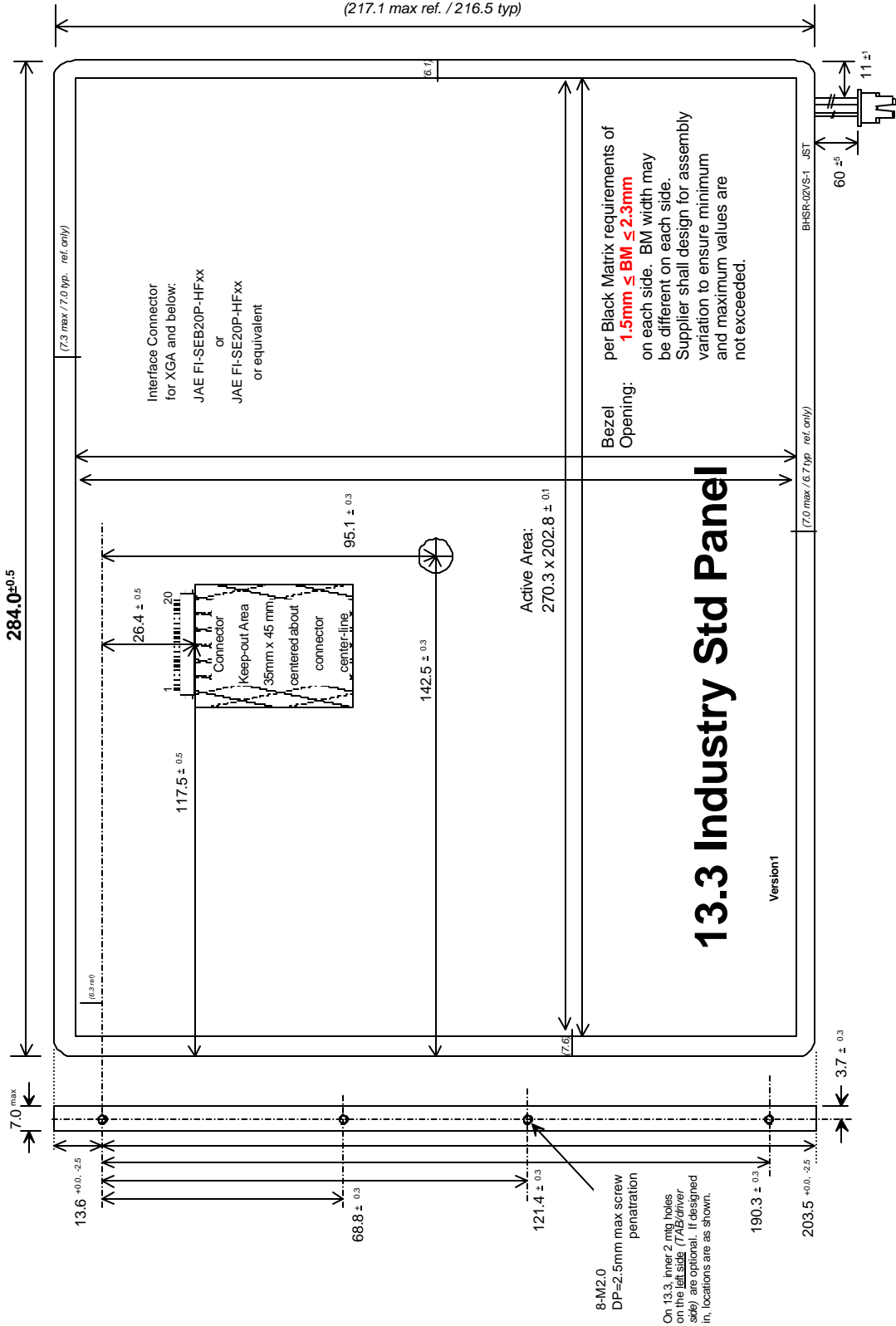
Figure 2 shows the pixel formatting for the active display surface. Figure's 3, 4, and 5 show the critical exterior dimensions for the 13.3", 14.1" and 15.0" panels.

**FIGURE 2**  
**XGA ACTIVE AREA PIXEL LAYOUT**





**FIGURE 3**  
**13.3" STANDARD PANEL CRITICAL DIMENSIONS**





**FIGURE 4**  
**14.1" STANDARD PANEL CRITICAL DIMENSIONS**

